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09/996,699	11/30/2001	Hiroshi Sakurai	NEG-234US	3647

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YOUNG & THOMPSON
745 SOUTH 23RD STREET 2ND FLOOR
ARLINGTON, VA 22202

EXAMINER	
NGUYEN, HOAN C	
ART UNIT	PAPER NUMBER
2871	

DATE MAILED: 06/17/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No. 09/996,699	Applicant(s) SAKURAI ET AL.	
	Examiner HOAN C. NGUYEN	Art Unit 2871	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *07 April 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1,3-5,7 and 8* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1,3-5,7 and 8* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

Applicant's arguments with respect to Amended claims 1, 3-5 and 7-8 based on the amendment filed on December 2, 2003 have been considered but are moot in view of the new ground(s) of rejection. Therefore, this is Final action.

Applicant cancelled claims 2, 6 and 9-16. Therefore, ONLY claims 1, 3-5 and 7-8 are pending.

In previous Non-Final Office Action, Claim 5 has indicated to contain the allowable subject matter, which is also held in this final office action.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

Claim 5 is rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01. The omitted steps are: "patterning of sequentially silicon layer 30, gate insulating film 40 and gate lines 51 on storage capacitor region" as Figs. 8a-e shown since the storage capacitor needs at least two electrodes, which are gate line 51 and a capacitor electrode 24. ONLY one capacitor electrode 24 as cited in claim 5 could not form the storage capacitor.

Claim R jections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

1. Claims 1 and 7-8 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (US5907008A) in view of Oki et al. (US5728592A) and Katsuya et al. (US6081310A).

Nakano et al. teach (Figs. 6 and 7) a process for producing reflection type liquid crystal display device, comprising the steps

(a) depositing resistance metal layer 34/35a on an insulating substrate, and using a first mask to pattern the metal layer to form source/drain electrodes;

(b) depositing a silicon layer 38, gate insulating film 40 and gate electrode layer 5a on said insulating substrate having said source/drain electrodes formed thereon in this order,

(c) depositing passivation film 41 on said insulating substrate having said source/drain electrodes, said thin film transistor region and said gate electrode formed thereon, and using third mask to form a first opening through said passivation film to said source electrode 34;

(d) depositing an interlayer insulating film 43 on said passivation film, and using a fourth mask to form a second opening through said interlayer insulating position corresponding to the first opening;

(e) depositing metal layer 42 over the surface of said interlayer insulating film to and electrically connected said source electrode through the first and second openings.

(f) treating at least said source/drain electrode with phosphine (PH_3) after said source/drain electrodes being formed and prior to successive deposition of said silicon layer, gate insulating film and gate electrode layer for forming an ohmic contact at the contacting portions (col. 28 lines 55-56) according to claim 8.

However, Nakano et al. fail to disclose a process for producing reflection type liquid crystal display device with

- using a second mask to pattern the silicon layer, the gate insulating film and gate electrode layer to form a thin transistor region;
- metal layer in step (e) to be reflective metal layer over the roughs surface of said interlayer insulating film.
- the step of heat treating at least the rough surface said interlayer insulating film before depositing said reflective metal and after forming the rough surface said interlayer insulating film (claim 7).

Oki et al. teach (Fig. 57a-58b) a process for producing reflection type liquid crystal display device, comprising the step of using a mask (the patterned resist film 113) to pattern the silicon layer110, the gate insulating film 111 and gate electrode

layer 112 to form a thin transistor region and gate electrode for simplifying structure and reducing cost (col. 1 lines 35-37).

Katsuya et al. teach (Fig. 7) a process for producing reflection type liquid crystal display device, comprising the step of depositing a reflective metal layer (silver/aluminum layer 14) over the rough surface of said interlayer insulating film 12 to form a reflection electrode extended and electrically connected to said source electrode through the openings 13 for conventionally diffusing reflection light (col. 11 lines 23-25).

In regard to claim 17, Katsuya et al. teach (Fig. 7, col. 13-16) a process for producing reflection type liquid crystal display device, comprising the step of heat treating at least the rough surface said interlayer insulating film before depositing said reflective metal and after forming the rough surface said interlayer insulating film for avoiding heat generation to reduce the light absorption of a reflecting surface (col. 2 lines 60-63).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a process for producing a reflection type liquid crystal display device as Nakano et al. with

- using a mask (the patterned resist film 113) to pattern the silicon layer110, the gate insulating film 111 and gate electrode layer 112 to form a thin transistor region and gate electrode for simplifying structure and reducing cost;

- depositing a reflective metal layer over the rough surface of said interlayer insulating film to form a reflection electrode extended and electrically connected to said source electrode through the openings for conventionally diffusing reflection light;
- heat treating at least the rough surface said interlayer insulating film before depositing said reflective metal and after forming the rough surface said interlayer insulating film for avoiding heat generation to reduce the light absorption of a reflecting surface.

2. Claims 3 and 4 are rejected under 35 U.S.C. 103(a) as being unpatentable over Nakano et al. (US5907008A) in view of Oki et al. (US5728592A) and Katsuya et al. (US6081310A) as applied to claims 1 and 8 above, and further in view of SUGITA et al. (US20030022071A1).

Nakano et al., Oki et al. and Katsuya et al. (US6081310A) fail to disclose the features in claims 3 and 4.

SUGITA et al. teach (Fig. 5) the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by halftone exposure or two-times exposure, wherein the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by using an exposure mask having transmissivity being controlled for carrying out overlay printing of a micro-line pattern (abstract lines 1-3).

Therefore, it would have been obvious to one having ordinary skill in the art at the time the invention was made to further modify a process for producing a reflection type liquid crystal display device as Nakano et al. with the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by halftone exposure or two-times exposure, wherein the formation of the rough surface of said interlayer insulating film and the opening for the transistor is conducted by using an exposure mask having transmissivity being controlled for carrying out overlay printing of a micro-line pattern.

Allowable Subject Matter

Claim 5 would be allowable if rewritten or amended to overcome the rejection(s) under 35 U.S.C. 112, second paragraph, set forth in this Office action.

The following is a statement of reasons for the indication of allowable subject matter: there is no prior art teaches a process for producing a reflection type liquid crystal display device shown in Figs. 8a-e comprising the steps of:

(f) forming a capacitor electrode 24 when said source/drain electrodes are formed;

(g) forming opening through said interlayer insulating film storage capacitor and said passivation film in position on said capacitor electrode when first and second openings are formed,

wherein

- the pattern of sequentially silicon layer 30, gate insulating film 40 and gate lines 51 on storage capacitor region;
- the reflection electrode extends through the third opening and is electrically connected to said capacitor.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Any inquiry concerning this communication or earlier communications from the examiner should be directed to HOAN C. NGUYEN whose telephone number is (571) 272-2296. The examiner can normally be reached on MONDAY-THURSDAY:8:00AM-4:30PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Kim H Robert can be reached on (571) 272-2293. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

HOAN C. NGUYEN
Examiner
Art Unit 2871

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ROBERT H. KIM
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800